



芯善科技

MPVD7N65

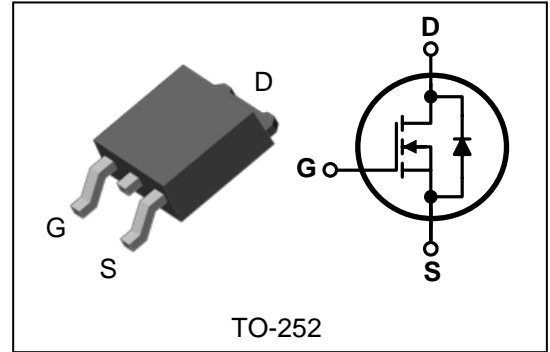
Power MOSFET

SWITCHING REGULATOR APPLICATIONS

Features

- Drain-Source breakdown voltage: $BV_{DSS}=650V$ (Min.)
- Low gate charge: $Q_g=20nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=1.35\ \Omega$ (Max.)
- 100% avalanche tested
- RoHS compliant device

PIN Connection



Ordering Information

ORDER CODE	MARKING	PACKING
MPVD7N65	MPVD7N65	TO-252

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V	650	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) *	I_D	$T_c=25^\circ C$	7.0	A
		$T_c=100^\circ C$	5.48	A
Drain current (Pulsed) *	I_{DM}	28	A	
Single avalanche current ^(Note 2)	I_{AS}	7.0	A	
Single pulsed avalanche energy ^(Note 2)	E_{AS}	245	mJ	
Repetitive avalanche current ^(Note 1)	I_{AR}	5.5	A	
Repetitive avalanche energy ^(Note 1)	E_{AR}	2.9	mJ	
Power dissipation	P_D	58	W	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55~150	$^\circ C$	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 4.27	$^\circ C/W$
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	



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MPVD7N65

Power MOSFET

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	3	4	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$			1.35	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=3.5\text{A}$	-	4	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	760	1046	pF
Output capacitance	C_{oss}		-	67	92	
Reverse transfer capacitance	C_{rss}		-	9	12	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=325\text{V}$, $I_D=7.0\text{A}$, $R_G=25\Omega$	-	55	128	ns
Rise time (Note 3,4)	t_r		-	79	174	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	94	208	
Fall time (Note 3,4)	t_f		-	33	75	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=7.0\text{A}$	-	20	-	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	4	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	7	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	7.0	A
Source current (Pulsed)	I		-	-	28	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=7.0\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=5.5\text{A}$, $V_{GS}=0\text{V}$ $di_F/dt=100\text{A}/\mu\text{s}$	-	494	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	2	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=15\text{mH}$, $I_{AS}=5.5\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Fig. 12 Gate Charge Test Circuit & Waveform

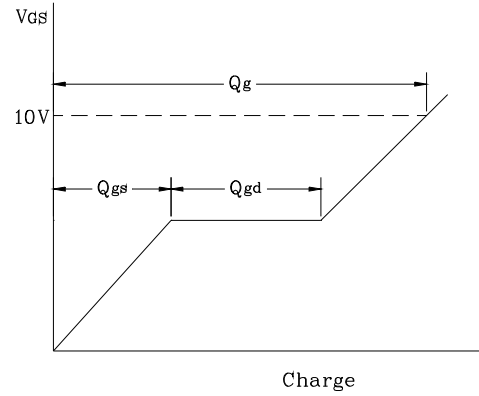
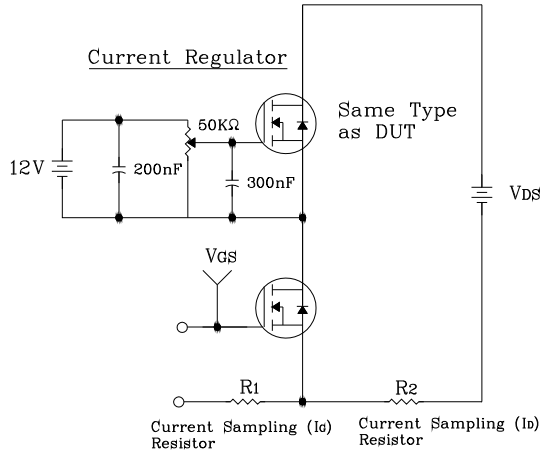


Fig. 13 Resistive Switching Test Circuit & Waveform

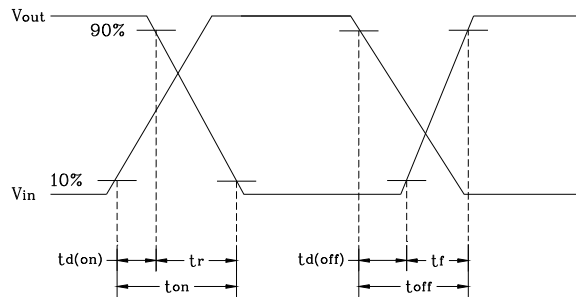
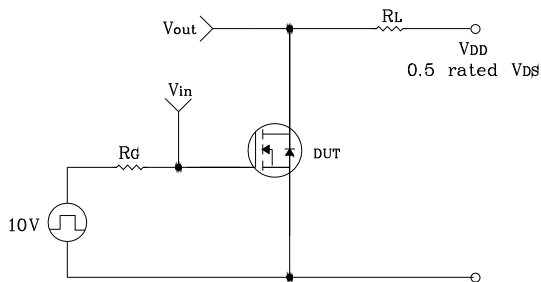


Fig. 14 E_{AS} Test Circuit & Waveform

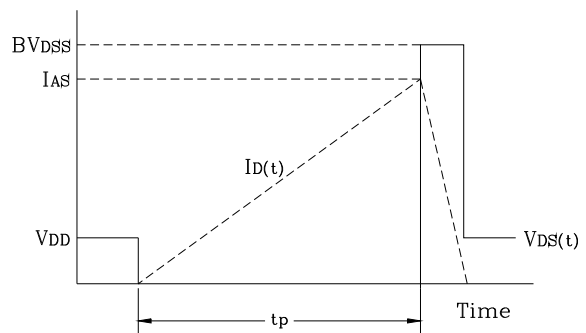
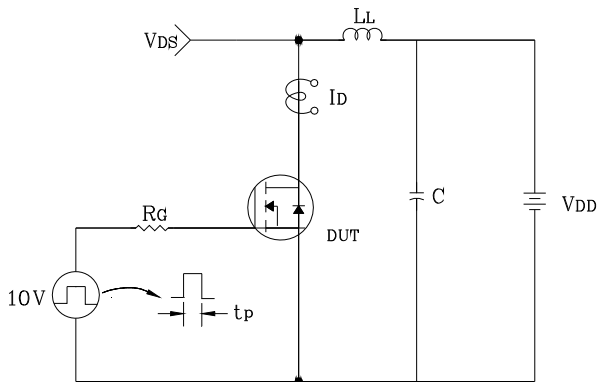
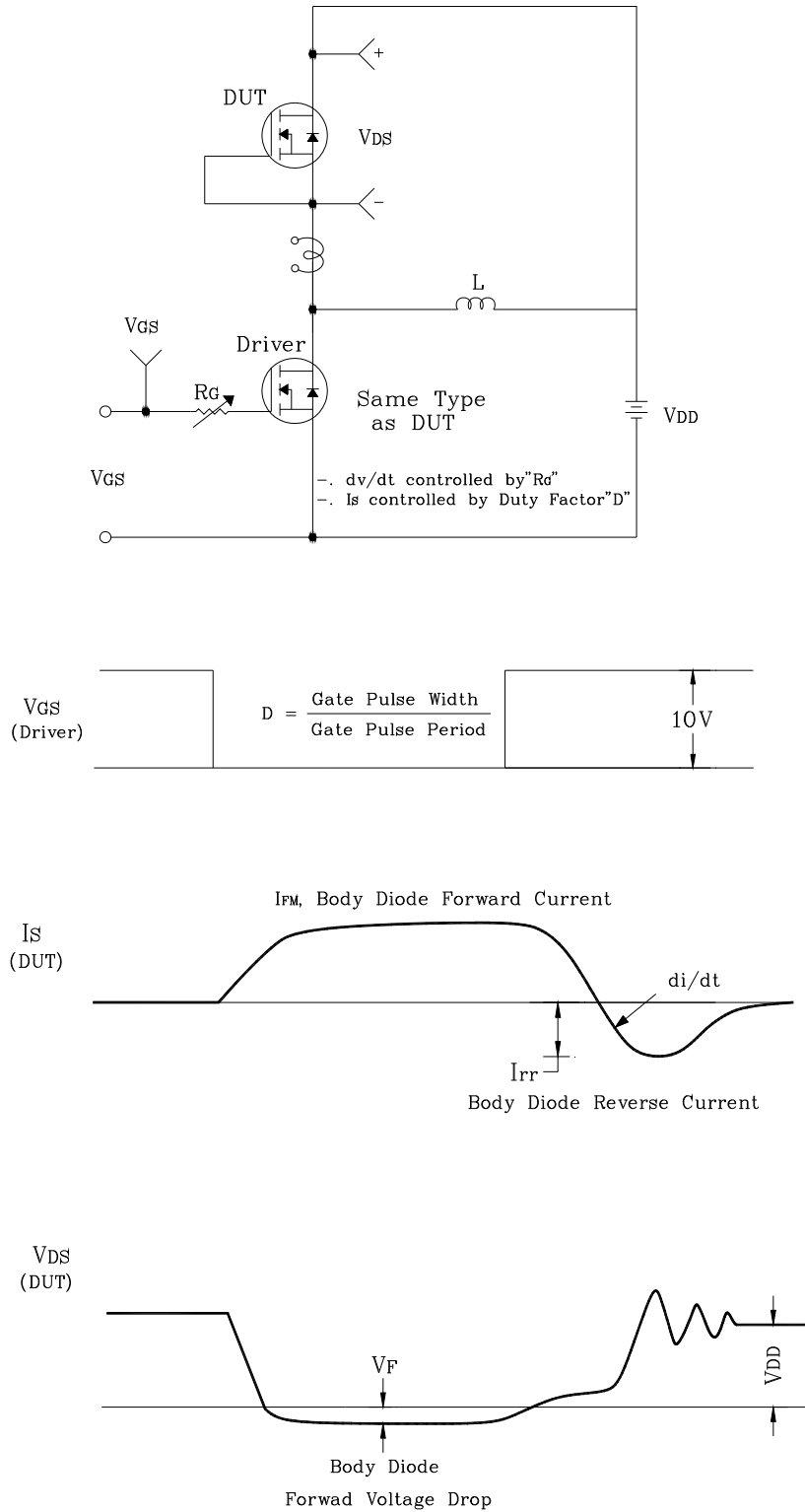


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



OUTLINE DIMENSION 产品尺寸图 (Unit: mm)

TO-252

